

## **AMENDMENTS TO THE DRAWINGS**

The attached sheet of drawings includes changes to FIG. 1. This sheet, which includes FIG. 1, replaces the original sheet including FIG. 1. In FIG. 1, previously omitted phrase "(PRIOR ART)" has been added.

Attachment:            Replacement Sheet

                         Annotated Sheet Showing Changes

### **REMARKS**

Claims 1-22 remain in the application. Claims 12-17 are allowed. Claims 1, 3, 5, 18 and 19 have been amended. Applicant respectfully requests allowance of each of pending claims 1-22.

#### **The Objections to the Drawings**

FIG. 1 is objected to for omitting a phrase "prior art." Such phrase has been added to FIG. 1 as shown in the replacement drawing sheet attached hereto. Thus, the objection is hereby overcome.

#### **The Objections to the Claims**

Claim 19 is objected to because of certain informalities. Claim 19 has been amended to replace ";" with "." at the end thereof. Thus, the objection is hereby overcome.

#### **The Rejections under 35 U.S.C. §112**

Claims 3-6 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 is rejected because the limitation "the transistors are N type, and the control voltage is coupled to the gate of transistor that is directly coupled to the high operating voltage" is not seen as recited in the present invention. Claim 3 has been amended as "the transistors comprise a first NMOS transistor directly coupled to the

high operating voltage and at least one second NMOS transistor serially coupled between the first NMOS transistor and the low voltage, the control voltage being coupled to a gate of the first NMOS transistor.” This particularly points out and distinctly claims the arrangement of the transistors and the control voltage which applicant regards as the invention. Thus, the rejection to claim 3 is hereby overcome.

Claim 4 is rejected as indefinite because of its dependency on claim 3. Since the amended claim 3 has overcome the 112 rejection, claim 4 is no longer indefinite. For reasons similar to the above, claims 5 and 6 are also definite under section 112.

#### **The Rejections under 35 U.S.C. §102**

Claims 1-2, 8, 10, 18-21 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,370,071 to Lall et al. (hereinafter referred to as “Lall”).

The independent claim 1 of the present invention is directed to a cascode device structure having one or more transistors of a same type connected in series and being operable with a normal operating voltage and a high operating voltage. One or more control voltages are controllably coupled to the gates of the transistors, wherein at least one of the control voltages coupled to the gate of at least one transistor is raised to a medium voltage level that is substantially higher than a normal operating voltage and lower than the high operating voltage.

Lall fails to teach such control voltage raised to a medium voltage level that is substantially higher than a normal operating voltage and lower than the high operating voltage.

Examiner asserts that, in FIG. 4, Lall teaches a control voltage (hvb) that is raised to a medium voltage ( $V_{pp}$  - threshold P1, P3) when transistor N1 is off (page 4). However, Applicant respectfully disagrees with such assertion. When signal En is low, which means transistor N1 is off, the signal hvb is at  $V_{pp}$ , not  $V_{pp}$  - threshold P1, P3 (col. 6, lines 29-33). If the signal hvb were  $V_{pp}$  - threshold P1, P3 when the signal En is low, both the PMOS transistors at the input stage 401 and the output stage 403 would have been turned on simultaneously, and generated conflicting signals. Since the signal hvb equals  $V_{pp}$  when transistor N1 is off, it is different from the control voltage as described in the claimed invention, which is substantially higher than a normal operating voltage and lower than the high operating voltage. In short, the signal hvb is not substantially lower than the high operating voltage, i.e.,  $V_{pp}$ .

As such, the independent claim 1 is not anticipated by Lall. Accordingly, claims 2, 8 and 10 that depend on the independent claim 1 are patentable over Lall as well.

For the same reasons discussed above, the independent claim 18 and its dependent claims 19-21 are patentable over Lall as well.

#### **The Rejections under 35 U.S.C. §103**

Claims 9 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lall. However, as discussed above, claims 9 and 11 depend on the independent claim 1 that cannot be anticipated by Lall. Thus, claims 9 and 11, which include all of the limitations set forth in the independent claim 1, are patentable over Lall as well.

### CONCLUSION

Applicant has made an earnest attempt to place this application in an allowable form. In view of the foregoing remarks, it is respectfully submitted that the pending claims are drawn to novel subject matter, patentably distinguishable over the prior art of record. The Examiner is therefore, respectfully requested to reconsider and withdraw the outstanding rejections.

Should the Examiner deem that any further clarification is desirable, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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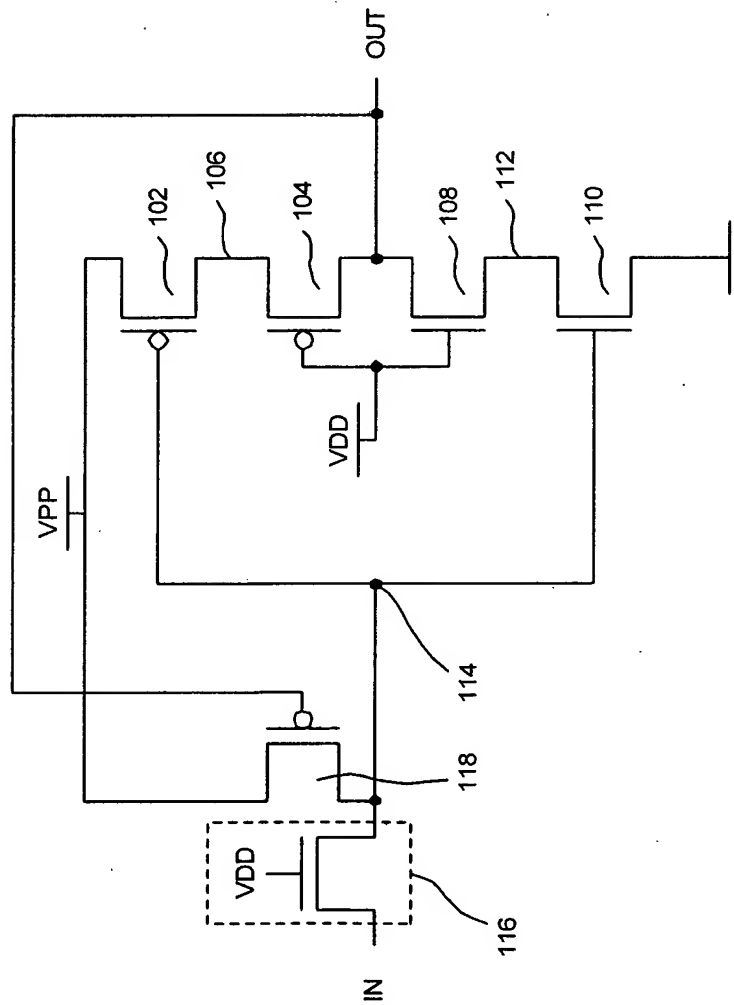


FIG. 1 (PRIOR ART)